REMARKS

Applicant respectfully requests the reconsideration of this application and the consideration of the following remarks.

The information disclosure statement filed 12/31/01 was objected to for not including a publication date for the reference "Proposed SMPTE Standard for Television, SMPTE314M". According to the web site of SMPTE (e.g., http://www.smpte.org/smpte_store/standards/index.cfm?scope=1&CurrentPage=13&stdtype=smpte), SMPTE314M was issued in 1999. Thus, applicant believes that the reference "Proposed SMPTE Standard for Television, SMPTE314M" was published in 1999 or earlier.

Claim 20 was objected to because of informalities. Claim 20 is currently amended to remove the informalities.

Claims 17-18, 20, 26-36 were rejected for insufficient antecedent basis for the term "the single instruction". Claims 17-18, 20 and 26 are currently amended to have/provide insufficient antecedent basis.

Claims 3-4 were rejected for using the term "substantially simultaneously". Applicant respectfully submits that a person skilled in the art understands the term "substantially simultaneously" in vector processing. Thus, the term "substantially simultaneously" is sufficient definite.

Claims 1-7, 10-18, 21-32 and 35-36 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,282,556 (hereinafter "Chehrazi"). Claims 8-9, 19-20, 33-34 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi in view of U.S. Patent No. 6,036,350 (hereinafter "Mennemeier").

Claim 1 is amended to include the limitation of claim 8 which is now canceled. Claim 1 recites:

1. (Currently Amended) A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

receiving a first plurality of numbers and a second plurality of numbers; and

generating a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers;

wherein the third plurality of numbers are saved in an entry in a register file;

wherein the above operations are performed in response to the microprocessor receiving the single instruction.

Applicant respectfully submits that claim 1 is patentable over Chehrazi in view of Mennemeier.

Chehrazi (e.g., Col. 20, line 42 – Col. 21, line 12) shows the sum of absolute differences (SABD) instruction. Figure 20B of Chehrazi clearly shows that the SABD instruction outputs the sum, not the vector of absolute differences. The SABD instruction as illustrated in Figure 20A shows two input registers (Vt and Vs) and only one destination register (Vd) (see also, Col. 20, lines 56-58, Chehrazi). Thus, no single instruction of Chehrazi computes a vector of absolute differences and outputs the vector of absolute differences in an entry of a register file.

Mennemeier shows a four-instruction execution process to compute the absolute differences (see, e.g., Col. 5, lines 9-10 and Figure 3 of Mennemeier), which uses a Packed Comparison For Greater Than Word (PCMPGTW) instruction, a Packed Exclusive-OR (PXOR) instruction, a Packed AND (PAND) instruction, and a Packed Subtraction (PSUBW) instruction. Thus, Mennemeier uses an instruction set very different from Chehrazi.

When viewed together, Chehrazi and Mennemeier show no indication of an arrangement in which a single instruction is used to compute and output absolute differences. Chehrazi showing a sum of absolute differences instruction that does not output absolute differences is a clear indication of non-obviousness.

Claims 12 and 26 recite limitations similar to that discussed above. Thus, claims 1, 12 and 26 are patentable over Chehrazi and Mennemeier.

Claim 23, for example, recites:

> 23. (Currently Amended) An execution unit in a microprocessor, the execution unit comprising:
> a first circuit configured to receive a first plurality of numbers;
> a second circuit configured to receive a second plurality of numbers; and
> a third circuit coupled to the first circuit and the second circuit, the third circuit, in response to the microprocessor receiving a single instruction, generating a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers
> wherein the microprocessor is a media processor <u>disposed on an integrated circuit with a memory controller</u>.

In rejecting claim 2, the Office Action pointed to item 100 of Fig. 1 and Col. 5, lines 46-54 of Chehrazi for the limitation of "a media processor *disposed on an integrated circuit with a memory controller*". Applicant respectfully disagrees.

In Chehrazi, item 100 of Fig. 1 is the bus (see, e.g., Col. 5, lines 43-45, Chehrazi). Col. 5, lines 46-54 of Chehrazi describes a computer system (112) with various components

connected to the bus (100). There is no indication that media coprocessor unit (108) is on an integrated circuit ***with a memory controller***.

Since neither Chehrazi or Mennemeier shows the limitation of "a media processor disposed on an integrated circuit with a memory controller", claims 2 and 23 and their dependent claims are patentable over the cited references.

Further, for example,

4. (Currently Amended) A method as in claim 2 further comprising:
testing if an overflow occurs in producing the first intermediate number and the second intermediate number;
saturating the absolute difference between the first number and the second number if an overflow occurs.

The Office Action rejected claim 4 based on the description of Col. 20, lines 9-18, Chehrazi, which is for Pack instructions. The Office Action asserted that the SABD instruction is a packed instruction based on Col. 20, lines 54-55 and argued that this description applies to the SABD instruction. Applicant respectfully disagrees.

The description of Col. 20, lines 9-18, Chehrazi relates to specific types of Pack instructions which converts 32-bit input operand into 16-bit output. There is no indication that the SABD is one of such instructions. In fact, a person skilled in the art can clearly see that the SABD instruction is not one of these Pack instructions. Further, Col. 20, lines 54-55, Chehrazi shows "the operands can be signed or unsigned packet bytes", which are not 32-bit input operands. Thus, the application of Col. 20, lines 9-18, Chehrazi to the limitation of claim 4 is improper.

Further, for example, new claims 37-39 recite:

37. (new) A method as in claim 1, wherein a type of each of the first and second pluralities of numbers is floating point number.

38. (new) A media as in claim 12, wherein the microprocessor is a media processor disposed with a memory controller on an integrated circuit.

39. (new) An execution unit as in claim 26 further comprising:
means for testing if an overflow occurs.

These limitations are not found in the cited references, either as indicated in the Office Action or as discussed above.

Please charge any shortages or credit any overages to Deposit Account No. 02-2666. Furthermore, if an extension is required, Applicant hereby requests such extension.

Respectfully submitted,

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